American International University- Bangladesh
Faculty of Engineering (EEE)
Analog Electronics Laboratory

Title: Study of MOSFET operations and characteristic curves.

Abstract:

A MOSFET transistor is a three terminal semiconductor device. To understand the operation of a MOSFET it is necessary to gather sufficient knowledge on MOSFET current-voltage or commonly known as I-V characteristics. This experiment describes the overview of MOSFET characterization that includes I-V characteristics, and determination of threshold voltage. In addition, the effect of source-substrate voltage on threshold voltage will be observed.

Introduction:

One of the most common transistor types is Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). BJTs based circuits used to dominate the electronics market in the 1960's and 1970's but nowadays most electronic circuits, particularly integrated circuits (ICs), are made of MOSFETs. As for the FET transistors, there are two main types: the junction field effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The power dissipation of a JFET based circuit would be simply too high. MOSFETs became the most popular field effect device in the 1980's. In this experiment, we will concentrate on the MOSFET transistor. We will investigate its characteristics and study its behavior when used as an amplifier or a switch. The objective of experiment is to become familiar with the characteristics and applications of Field Effect Transistors (MOSFETs) such as --.

1. To understand the operation of the MOSFET and determine the threshold voltage.
2. To measure the I-V characteristics and find the different operating regions.
3. To obtain MOSFET transfer characteristic curves.

Theory and Methodology:

MOSFETs Structure and Physical Operation

The MOSFETs are the most widely used FETs. Strictly speaking, MOSFET devices belong to the group of Insulated Gate Field Effect Transistor (IGFETs). As the name implies, the gate is insulated from the channel by an insulator. In most of the cases, the insulator is formed by a silicon dioxide (SiO_2), which leads to the term MOSFET. MOSETs like all other IGFETs have three terminals, which are called Gate (G), Source (S), and Drain (D). In certain cases, the transistors have a fourth terminal, which is called the bulk or the body terminal. In PMOS, the body terminal is held at the most positive voltage in the circuit and in NMOS, it is held at the most negative voltage in the circuit.

There are four types of MOSFETs: enhancement n-type MOSFET, enhancement p-type MOSFET, depletion n-type MOSFET, and depletion p-type MOSFET. The type depends whether the channel between the drain and source is an induced channel or the channel is physically implemented and whether the current owing in the channel is an electron current or a hole current. If the channel between the drain and the source is an induced channel, the transistor is called enhancement transistor. If the channel between the drain and source is physically implemented then the transistor is called depletion transistor. If the current owing in the channel is an electron current, the transistor is called an n- type or NMOS transistor. If the current flow is a hole current then the transistor is called p-type or PMOS transistor. Throughout the handout we will concentrate on analyzing the enhancement type MOSFET. The cross section of an enhancement NMOS transistor is shown in figure 1. If we put the drain and source on ground potential and apply a positive voltage to the gate, the free holes (positive charges) are repelled from the region of the substrate under the gate (channel region) due to the positive voltage applied to the gate. The holes are pushed away downwards into the substrate leaving behind a depletion region. At the same time, the positive gate

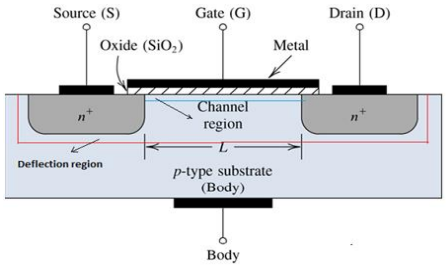


Figure 1: Schematic cross section of an enhancement-type NMOS transistor

voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is higher than the concentration of holes, an n region is created, connecting the source and the drain regions. The induced n-region thus forms the channel for current flow from drain to source voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is higher than the concentration of holes, an n region is created, connecting the source and the drain regions. The induced n-region thus forms the channel for current flow from drain to source. The channel is only a few nanometers wide. Nevertheless, the entire current transport occurs in this thin channel between drain and source. Now if a voltage is applied between drain and source electrodes an electron current can flow through the induced channel. Increasing the voltage applied to the gate above a certain threshold voltage enhances the channel. In the case of an enhancement type NMOS transistor the threshold voltage is positive, whereas an enhancement type PMOS transistor has a negative threshold voltage. So, in order for the current to flow from drain to source, the condition that should be satisfied is $V_G > V_{th}$, where V_G is the gate voltage and V_{th} is the minimum voltage required to form a channel between drain and source so that carriers can ow through the channel. By changing the applied gate voltage, we can modulate the conductance of the channel.

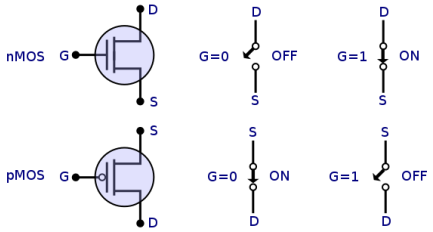


Figure 2: Symbols for Enhancement NMOS and PMOS transistors

NMOS Transistor

MOSFET I-V Characteristics

MOSFET I-V characteristics depend on the voltage supplied to the drain terminal. There are two possibilities, one is small signal operation and another one is large signal operation. If drain voltage is very small (in mv range), the characteristics can be represented by the Ohm's Law. That means it shows the linearity. Since V_{DS} is kept small the transistor acts as a resistor with a value that is determined by the gate voltage, if this voltage is 0.2V so that the transistor will act as an electronically controlled resistor. Figure 3 shows the MOSFET circuit that used to analyze the I-V characteristics I-V characteristics.

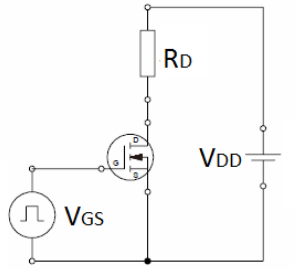
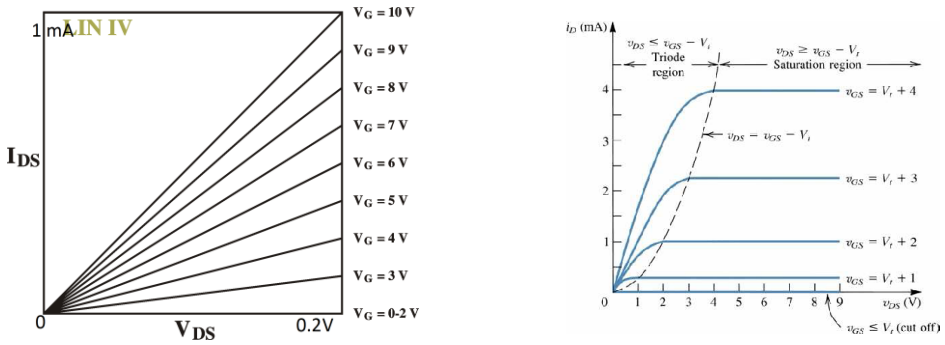


Figure 3: MOSFET circuit

Figure 4a shows the I-V characteristics of MOSFET circuit when V_{DS} is very small. Now if drain voltage is gradually increased the output curves will not show the linearity it becomes non-linear. Therefore for the large

signal operation is established, we will introduce now the description of the I-V characteristics of enhancement n-type MOSFETs when drain voltage is high. The output curves of an enhancement n-type MOSFET are shown in figure 4b.



(a) (b)

Figure 4: Output curves of an n-type enhancement MOSFET when (a) V_{DS} is small (b) V_{DS} is large.

The drain current I_D is shown as a function of drain source voltage, V_{DS}. The drain current is shown for different gate voltage V_{GS}. Based on the output curves three different device regions of operation can be distinguished: cut-off region, linear (triode) region, and saturation region. Digital circuits usually make excursions into all three regions, whereas analog circuits such as amplifiers typically only use the saturation region.

MOSFET Regions of Operation

In order for the MOSFET to work in any of the three regions, some conditions should be satisfied which in turn control the performance of the transistor, as follows:

Cut-off Region

MOSFETs are in the cut-off region when there is no current flow between source and drain terminals. This happens when the gate-to-source voltage is less than the threshold voltage, i.e., $V_{GS} < V_{th}$.

Triode region

For voltages higher than the threshold voltage, the transistor operates in the linear or triode region if at the same time the voltage V_{DS} is smaller than $V_{GS} - V_{th}$. In this case, the current flow is a function of both gate-to-source voltages higher than the threshold voltage. When the drain to source voltage V_{DS} is smaller than V_{GS}-V_{th}, the transistor operates in the triode region. The currents-voltage relationship is given by,

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{when } v_{DS} < (v_{GS} - V_t)$$

The parameter $k_n' = \mu_n C_{ox}$ is the trans conductance parameter, μ_n is the mobility, C_{ox} is the capacitance of the oxide layer and W/L is the ratio of the channel (or gate) width over length. Notice that when V_{DS} is much smaller than $V_{GS} - V_{th}$, the current can be approximated as follows,

$$i_D \approx k_n' \frac{W}{L}(v_{GS} - V_t)v_{DS} \qquad \text{when} \quad v_{DS} << (v_{GS} - V_t).$$

Thus the transistor acts as a voltage-controlled resistor whose value is given by (provided that $v_{GS} > v_{th}$),

$$r_{DS} = \frac{1}{k_n' \frac{W}{L}(v_{GS} - V_t)}$$

Saturation region

When the drain to source voltage exceeds the value $V_{GS} - V_{th}$, the channel will be pinched off and the current can be written as-

$$i_D = \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - V_t)^2 \qquad \text{when } v_{DS} > (v_{GS} - V_t)$$

In the expression above, the drain current is independent of the drain-source voltage what implies that the transistor acts as an ideal current source in this region. This is only an approximation. In reality, the current will vary slightly with the drain voltage. This variation can be modeled by adding a parameter λ, called the channel length modulation parameter, as shown in the following expression,

$$i_D = \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \qquad \text{when } v_{DS} > (v_{GS} - V_t)$$

The channel length modulation parameter λ is usually pretty small (typical values are 0.02 V^{-1}). The output resistance of the transistor in saturation can now be written as,

$$r_o = \frac{1}{I_D \lambda} = \frac{V_A}{I_D}$$

where I_D is the drain current, and V_A (=1/λ) is the Early voltage.

PMOS transistor

The **PMOS** transistor has similar characteristics. The only difference is that the polarity of the voltages changes, as shown in Figure 5.

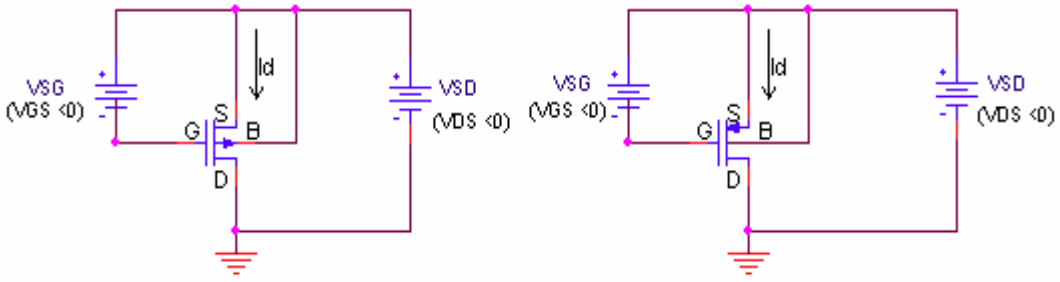


Figure 5: PMOS transistor showing two symbols and direction of the current flow.

The values of the threshold voltage V_t (for enhancement transistor), and of λ and kp' are now negative. The current expressions are then given by,

Triode Region:

$$i_D = k_p' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{when } v_{DS} > (v_{GS} - V_t)$$

Saturation Region:

$$i_D = \frac{1}{2} k_p' \frac{W}{L} (v_{GS} - V_t)^2 \qquad \text{when } v_{DS} < (v_{GS} - V_t)$$

If can takes into account the channel length modulation, the current is given by

$$i_D = \frac{1}{2} k_p' \frac{W}{L} (v_{GS} - V_t)^2 (1 + \lambda v_{DS}) \qquad \text{when } v_{DS} < (v_{GS} - V_t)$$

Threshold Voltage

It is important to note that the threshold voltage Vth of MOSFETs can be controlled by the fabrication process and can be made either positive or negative for both types of MOSFETs. In the case of enhancement type transistors the channel is formed (induced) by the applied gate voltage and the threshold voltage is defined in the following way:

- Enhancement type NMOS: $V_{th} > 0$
- Enhancement type PMOS: $V_{th} < 0$

Pre-Lab Homework:

1. Explain the differences between an enhancement and depletion type MOSFET.

2. Explain the differences between an NMOS and PMOS transistor.

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

Hints: to determine the transfer characteristics V_{DS} should be scanned from 0 to 7V and V_{GS} should be scanned from +3 to +6V.

Apparatus:

(1) Resistors: 470 Ohms 1pcs
(2) NMOS
(3) Connecting wires and DC supply probes
(4) Multimeter
(5) Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Simulation:
Do the simulation using a convenient software (Multisim is recommended). Observe NMOS transfer and output characteristic curves. Attach your simulation results with your report.

Experimental Circuit:

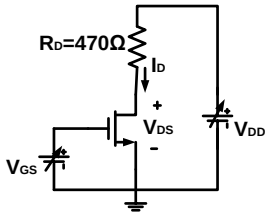


Figure 6: Basic NMOS circuit for observing its operation and characteristics.

Experimental Procedure:

Problem 1: Determination of Threshold Voltage (V_{th})

The purpose of this part of experiment is to determine the threshold voltage of NMOS. Threshold voltage is the minimum required voltage by a MOSFET to begin the operation.

1. Construct the circuit as shown in figure 6 to determine V_{th}.
2. By keeping V_{DD}=5V change V_{GS} from 0V to 5V and measure V_{DS} and I_D.
3. Complete the following table 1.

Table 1 Determination of NMOS Threshold Voltage

V_{GS}	V_{DS}	I_D
0		
1		
2		
3		
4		
5		

4. Now short gate and drain which implies that $V_{th} = V_{GS} = V_{DS}$. Record following values.

$V_{GS} = V_{th}$	I_D=	V_{DS}=

Problem 2: Determination of Transfer Characteristic Curve

1. Use the same circuit to measure the transfer characteristic (Don't short G and D).
2. Make that V_{DD} is kept constant at 5V constant and scan V_{GS} from 0V to 7V.
3. Record the changes in V_{DS} for every change in V_{GS} and complete the following table 2.

Table 2: V_{DS} and V_{GS} values for transfer characteristic curve

V_{GS}	V_{DS}
0	
1	
2	
3	
4	
5	
6	

4. Draw the transfer characteristic curve and identify the operating regions on the curve

Problem 3: Determination of NMOS I-V Characteristic Curve or Output characteristic curve

1. Use the same circuit and measure the output characteristic for gate source voltages.
2. Keep gate to source voltage at 2V and change drain source voltage from 0V to 4V.
3. Record I_D current for every V_{DS} value.

4. Repeat 1 to 3 for V_{GS}= 3V, 3.4V, and 3.6V.
5. Complete the following table 3.

Table 3 Data for output characteristic curve

V_{GS}= 2V		V_{GS}= 3V		V_{GS}= 3.2V		V_{GS}= 3.6V	
V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D
0		0		0		0	
1		1		1		1	
2		2		2		2	
3		3		3		3	
4		4		4		4	

6. Draw the I-V characteristic curve and identify the operating regions on the curve

Results and Discussion:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Report:

1. Plot the measured transfer characteristic.
2. Plot the measured output characteristic for the different gate source voltages.
3. Insert the $V_{DS} = V_{GS} - V_{th}$ line into the output characteristic.
4. Explain the phase relationship between input and output signals of MOSFET amplifier.

Reference(s):

1. A.S. Sedra, K.C. Smith, Microelectronic Circuits, Oxford University Press (1998).
2. J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001).
3. P. Horowitz, W. Hill, The Art of Electronics, Cambridge University Press (1989).
4. David Comer & Donald Comer, "Fundamentals of Electronic Circuit Design".