American International University- Bangladesh
Faculty of Engineering (EEE)
Analog Electronics Laboratory

Title:

Determination of Threshold Voltage, Output Resistance, and process technology parameters of a MOSFET

Abstract:

The most common commercial transistor today is the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). Even though the MOSFET was conceived before the bipolar transistor, it wasn't until mature fabrications techniques and the digital revolution that the MOSFET became the dominant transistor used today. Even though the MOSFET has been primarily used as a digital device, it has made significant contributions to analog circuit design in recent times despite its relatively poor trans conductance compared to the Bipolar Junction Transistor (BJT), primarily due to the needs for mixed signal circuit driven by integration of multiple functions on a single IC. The objective of this laboratory is to analyze the properties of an enhancement type of MOSFET that significantly dominates the operation of the MOSFET. In this experiment student are meant to find the threshold voltage, output resistance, and process technology parameters for both the p-type and n-type MOSFETs.

Introduction:

Analysis of MOSFET circuits is based on three possible operating modes: cutoff, triode, and saturation. In cutoff, the gate-to-source voltage is not greater than the threshold voltage, and the MOSFET is inactive. In triode, the gate-to-source voltage is high enough to allow current flow from drain to source, and the nature of the induced channel is such that the magnitude of the drain current is influenced by the gate-to-source voltage and the drain-to-source voltage. As the drain-to-source voltage increases, the triode region transitions to the saturation region, in which drain current is (ideally) independent of drain-to-source voltage and thus influenced only by the physical characteristics of the FET and the gate-to-source voltage. The saturation-region relationship between gate-to-source voltage (V_{GS}) and drain current (I_D) is expressed as follows:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$$

The transition to saturation mode occurs because the channel gets "pinched off" at the drain end. Unfortunately, the "pinching off" isn't the end of the influence exerted by the drain-to-source voltage. Further increases continue to affect the channel because the pinch-off point moves closer to the source. The resistance of the channel is proportional to its width-to-length ratio; reducing the length leads to decreased resistance and hence higher current flow. Thus, channel-length modulation means that the saturation-region drain current will increase slightly as the drain-to-source voltage increases. The incremental channel-length reduction is added into the original expression as follows:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{(L-\Delta L)}(V_{GS}-V_{TH})^2 \quad \text{and} \quad I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{(L-\Delta L)}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

Now we just need to come up with a parameter that accounts for how a certain semiconductor process technology responds to changes in the drain-to-source voltage. Here, λ is the measure of channel length modulation. Due to this phenomenon of a MOSFET the output resistance at saturation region has a finite value.

Theory and Methodology:

Threshold Voltage:

The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region of a enhancement type MOSFET to form a conducting channel is called the threshold voltage and is denoted V_t . The value of V_t is controlled during device fabrication and typically lies in the range of 0.3 V to 1.0 V.

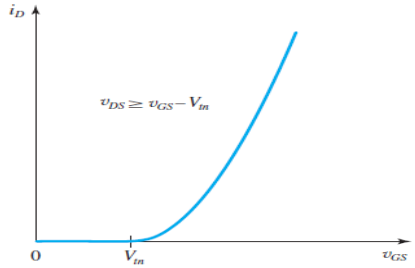


Figure 1: Drain current I_D vs gate to source voltage V_{GS} graph of an enhancement type NMOS showing threshold voltage V_{tn}

In case of enhancement type transistors the channel is formed (induced) by the applied gate voltage and the threshold voltage is defined in the following way:

Enhancement type NMOS: $V_{tn} > 0$
Enhancement type PMOS: $V_{tp} < 0$

In the case of a depletion type transistor the channel is already physically implementedby doping the region so that already a drain current can flow for VGS = 0V.

Depletion Mode NMOS: $V_{tn} < 0$
Depletion Mode PMOS: $V_{tp} > 0$

A MOSFET can operate in any of the three regions: cut-off, triode and saturation.

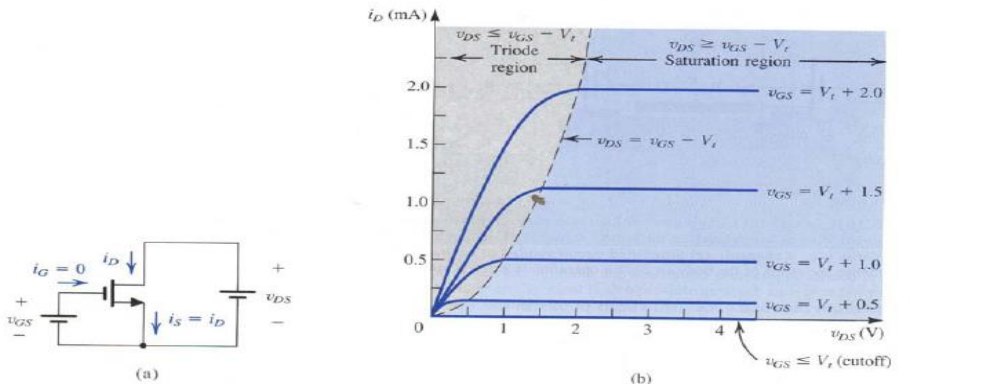


Figure 2: (a) an n-channel enhancement type MOSFET with v_{GS} and v_{DS} applied (b) the $i_D - v_{DS}$ characteristics of a device with $k'_n(W/L) = 1$ mA/V^2 showing the three operating region

For NMOS:

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{when } v_{DS} < (v_{GS} - V_t)$$

[Triode region]

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2 \qquad \text{when } v_{DS} > (v_{GS} - V_t)$$

[Saturation region without considering channel length modulation]

$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \qquad \text{when } v_{DS} > (v_{GS} - V_t)$$

[Saturation region considering channel length modulation]

For PMOS:

$$i_D = k_p' \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right] \qquad \text{when } v_{DS} > (v_{GS} - V_t)$$

[Triode region]

$$i_D = \frac{1}{2}k_p' \frac{W}{L}(v_{GS} - V_t)^2 \qquad \text{when } v_{DS} < (v_{GS} - V_t)$$

[Saturation region without considering channel length modulation]

$$i_D = \frac{1}{2}k_p' \frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \qquad \text{when } v_{DS} < (v_{GS} - V_t)$$

[Saturation region considering channel length modulation]

MOSFET Parameters:

NMOS:

V_{tn} = Threshold voltage for a NMOS [V]
W = Width of the transistor [µm]
L = Channel-length [µm]
λ_n = Channel-length modulation factor [V^{-1}]
$K'_n = \mu_n C_{ox}$ = Transconductance coefficient [A/V^2]
C_{ox} = Gate capacitance per unit area [F/m^2]
t_{ox} = Oxide layer thickness [µm]
ε_{ox} = Permittivity of the oxide (3.9)*8.85E-14 [F/cm]

PMOS:

V_{tp} = Threshold voltage for a NMOS [V]
W = Width of the transistor [µm]
L = Channel-length [µm]
λ_p = Channel-length modulation factor [V^{-1}]
$K'_p = \mu_p C_{ox}$ = Transconductance coefficient [A/V^2]
C_{ox} = Gate capacitance per unit area [F/m^2]
t_{ox} = Oxide layer thickness [µm]
ε_{ox} = Permittivity of the oxide (3.9)*8.85E-14 [F/cm]

Channel-length modulation factor λ can be measured as: $\lambda = 1/V_A$, where V_A is called the early voltage and it is a process technology parameter normally given in the datasheet.

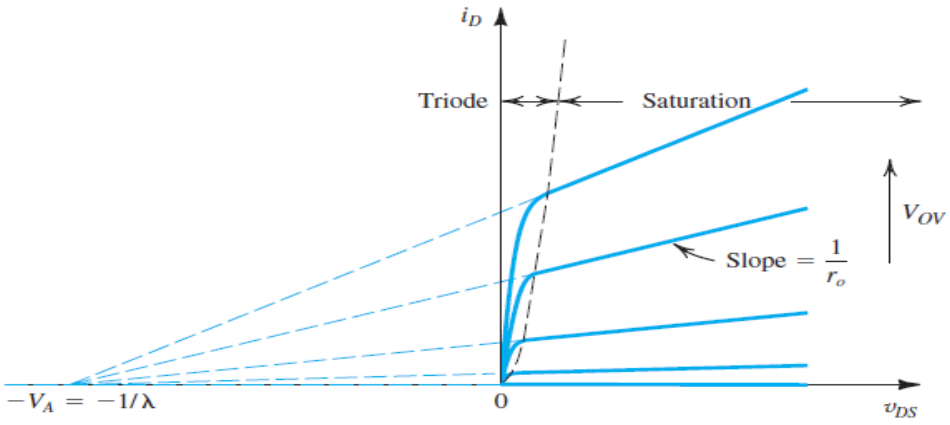


Figure 3: Calculation of λ from $i_D - v_{DS}$ characteristics of an NMOS

Output Resistance:

Due to channel length modulation, the MOSFET has a finite output resistance in saturation region. The output resistance of a MOSFET in saturation region is given by:

$$r_o = \frac{1}{\lambda I_D}$$

Where, I_D is the drain current without considering channel length modulation and is given by:

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{tn})^2$$

Pre-Lab Homework:

1. Define all the parameters of a MOSFET.
2. Explain channel length modulation and its effect on the operation of a MOSFET.

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

Apparatus:

(1) Multimeter
(2) NMOS
(3) PMOS
(4) Connecting wires
(5) Trainer Board
(6) 1kΩ resistor

Precautions:

MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do not touch any of the pins of the chip.

Experimental Procedure:

1. Connect the circuits as shown in Fig. 1 and Fig. 2.
2. Place an ammeter in Box 1. Slowly increase the voltage at V_{CC} until you see current start to flow. This is the point where the transistor has transitioned from cutoff to saturation region. Estimate V_{tp}.
3. Add a 1kΩ resistor in series with the ammeter. Use V_{CC} = 5V. Measure V_{DS} and I_D of the transistor. Use the saturation current equation to determine $K_p = K'_p(W/L)$.
4. Repeat step 1 and 2 for NMOS as in fig. 2 to find V_{tn} and K_n.

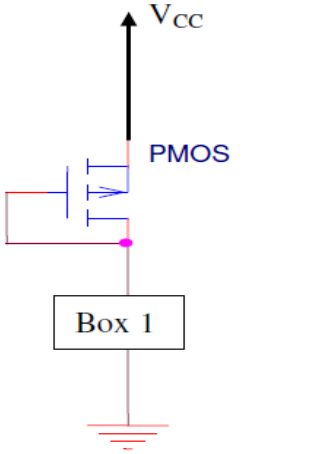


Figure 1. Measurement circuit to determine V_{tp} and K_p for p-type MosFets

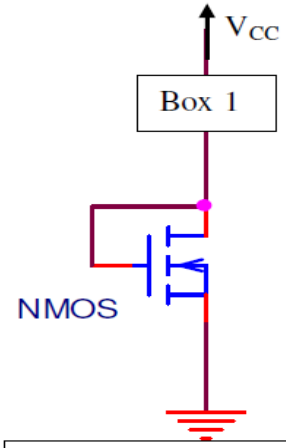
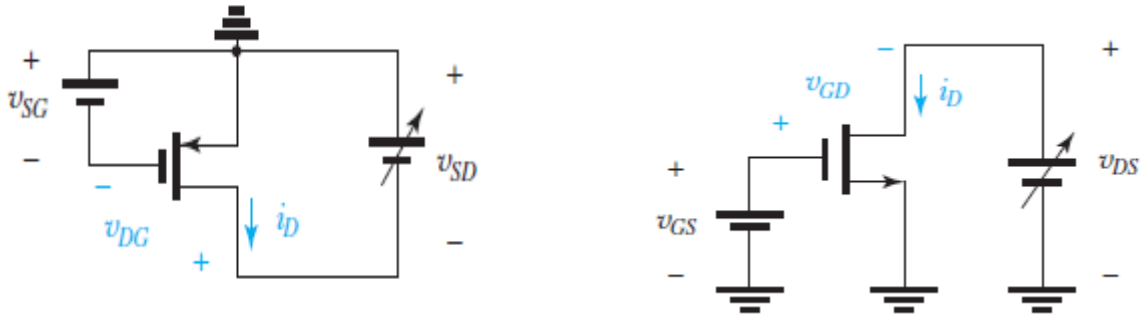


Figure 2. Measurement circuit to determine V_{tn} and K_n for n-type MosFets

5. Connect the circuit as shown in fig. 5(a) for PMOS and fig. 5(b) for NMOS.



(a) (b)

Figure 5: Circuit for drawing $i_D - v_{DS}$ curve for (a) PMOS and (b) NMOS

6. Keep V_{GS} fixed at 5 V. Now vary V_{DS} from 0-16 volts and measure corresponding I_D. Fill up table 1.
7. Plot the $i_D - v_{DS}$ curve and find λ as shown in fig. 3 for both PMOS and NMOS.
8. Calculate output resistance using:

$$r_o = \frac{1}{\lambda I_D}$$

Table 1: Data to plot $i_D - v_{DS}$ curve

SL.	V_{DS}	I_D
1	0	
2	2	
3	4	
4	6	
5	8	
6	10	
7	12	
8	14	
9	16	

Simulation and Measurement:

Match your simulated results from the "Pre-lab Homework" section with your practical results.

Results and Discussion:

Summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Question/Answer:

1. Explain Channel length modulation and its effect on MOSFET operation.
2. Discuss MOSFET resistance in triode and saturation regions.

References:

1. Adel S. Sedra, and Kenneth C. Smith, "Microelectronic Circuits,"
2. Integrated Electronics: Analog and Digital Circuits and Systems by Jacob Millman, Christos
3. J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001).