Title:	Design of a Multipurpose Ternary Arithmetic Circuit Using CNTFET
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Published Journal Name:	Journal of Semiconductor Devices and Circuits
Type of Publication:	Journal
Volume:	3 Issue 1
Publisher:	STM Journals
Publication Date:	2016
ISSN:	2455-3379
URL:	https://engineeringjournals.stmjournals.in/index.php/JoSDC/article/view/2077
Other Related Info.:	Page 13-24

Citation: Kazi Muhammad Jameel, Mohammad Abdul Mannan, Md. Tanvir Hasan, "Design of a Multipurpose Ternary Arithmetic Circuit Using CNTFET", Journal of Semiconductor Devices and Circuits (STM Journals), Vol. 3, Issue 1, pp. 13-24, 2016.

Abstract:

In this paper, a multipurpose ternary arithmetic circuit is presented for ternary processors based on carbon nanotube field effect transistors (CNTFETs). Both addition and subtraction can be performed using same circuit's configuration, which is the special feature of the proposed circuit. The combination of pseudo and complimentary logic structure are employed to blend the binary and ternary logic techniques. The propagation delay and power delay product are 139.5 pico second and 3.18 femto Joule, which indicates significant improvement in power consumption, delay and PDP, compared to few recent ternary full adder designs.

Keywords: Ternary arithmetic circuits, ternary full adder, TFA, ternary full subtractor, TFS