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| **Abstract:** |  |
| Abstract—This research paper presents a comprehensive comparative analysis of the 4×4 multiplier design of Wallace, Braun array, and Vedic architectures constructed through Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology using both 45 nm and 90 nm processes of the Cadence tool. Furthermore, the best-performing architecture is then built using Gate Diffusion Input (GDI) and Transmission Gates (TG) to compare the performance matrices to those of CMOS technology. The study investigates and compares these technologies’ design processes and key parameters, focusing on critical metrics, such as power consumption, area efficiency, propagation delay, and operating clock frequency. By extending its analysis, the paper compares the performance parameters of various multiplier circuits built using these technologies with the previous research findings, highlighting the advancements and efficiency improvements. The Cadence simulation results demonstrate the competitive advantages and trade-offs inherent in each technology, offering valuable guidance for designers in selecting the most suitable approach for multiplier implementations in digital systems. | |