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| **Title:** | Design, Simulation and Comparative Analysis of Performance Parameters of a 4-bit CMOS based Full Adder Circuit using Microwind and DSch at Various Technology Nodes | | |
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| **Published Journal Name:** | IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) | | |
| **Type of Publication:** | Journal | | |
| **Volume:** | 11 | Issue | 1 |
| **Publisher:** | IOSR | | |
| **Publication Date:** | January-February 2021 | | |
| **ISSN:** | e-2319-4200, p-2319-4197 | | |
| **DOI:** | 10.9790/4200-1101010108 | | |
| **URL:** | https://www.iosrjournals.org/iosr-jvlsi/papers/vol11-issue1/ | | |
| **Other Related Info.:** | pp. 1-8, IF=2.82, Google Scholar and Research Gate Indexed | | |
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| **Abstract:** |  |
| Abstract— For any kind of digital circuit, decreasing of surface area is one of the crucial factors. Very Large Scale Integration (VLSI) technology is used to diminish the chip area to increase packing density as well as to increase performances. Full adder circuit is a digital circuit that is one of the important components in computer or any kind of processor for arithmetic operation. Now 64-bit arithmetic operations are being performed. Therefore, we need huge amount of area to perform this operation. Not only that, we need to reduce power consumption, noise margin but at the same time to increase speed of operation. Reducing the transistor size can provide us such benefits even we increase number bits to be handled in parallel. In this paper, design and simulation of a 4-bit CMOS based full adder circuit at various technology nodes using Microwind and DSch are presented. After that performances are compared to see how the reduction of transistor size can help to achieve those benefits. The designed circuit is used for the addition of 4-bit binary numbers. To design 4-bit full adder fully automatic CMOS design process is used. In the first fully CMOS design, schematic and layout of 4-bit full adder is developed. The layouts are designed and simulated at 90 nm, 65 nm and 45 nm technology nodes. It has been observed from the simulated results and various outputs that the reduction of node sizes improves the performances of the digital integrated circuit. | |