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| **Title:** | A Review of the Fabrication Process of the Pocket Implanted MOSFET Structure | | |
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| **Abstract:** |  |
| Abstract— The dimensions of the various types of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device structures are being shrunk continuously to accommodate more transistors inside a single chip. However, these shrinking entail several impacts on the device performance degradation and hence it has become cumbersome to operate the device properly at its various biasing conditions. To obtain the best performance from the shorter device, the modified device structure is being proposed or developed by the device design engineers. One such effort is to have the additional dopant atoms laterally at the channel region’s drain and/or source sides through the ion implantation process. This is known as pocket implantation and the new device structure thus obtained is called pocket implanted MOSFET. Due to this extra doping, the threshold voltage is increased rather than decreased as the channel length is reduced. This new effect is termed the Reverse Short Channel Effect or in short RSCE. However, the new device structure requires new fabrication processes. Therefore, in this paper, the formation processes of the pocket structure have been described in detail by studying the various literature. To fabricate the pocket implanted Metal Oxide Semiconductor Field Effect Transistor (MOSFET) structure, we require several fabrication steps, like, Chemical Vapor Deposition (CVD), Ion Implantation, Electron Beam Lithography (EBL), Rapid Thermal Annealing (RTA), Reactive Ion Etching (RIE), etc. All these steps are described herein brief so that a clear picture can be obtained about it The knowledge of these steps can be utilized to derive the various operational parameters, such as surface potential, threshold voltage incorporating bias and temperature effects, effective mobility model, subthreshold drain current, drain current flicker noise, etc. of the pocket implanted n-MOSFET device as well as their modeling and characterization. | |