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| **Title:** | Design and Implementation of FPGA based 32-bit Carry Look Ahead Adder using Verilog HDL in Xilinx Environment | | |
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| **Published Journal Name:** | Journal of Bangladesh Electronics Society | | |
| **Type of Publication:** | Journal | | |
| **Volume:** | 9 | Issue | 1-2 |
| **Publisher:** | Bangladesh Electronics and Informatics Society | | |
| **Publication Date:** | December 2009 | | |
| **ISSN:** | p-1816-1510 | | |
| **DOI:** |  | | |
| **URL:** | http://beis.org.bd | | |
| **Other Related Info.:** | pp. 161-167 | | |
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| **Abstract:** |  |
| Abstract— This paper presents the design method and simulation strategy of a 32-bit carry look ahead adder using verilog HDL. To implement this large adder,2-bil and 4-bit adder blocks are used separately. The carry signals are generated using the logic equations in verilog HDL. The verilog HDL design is verified using ModelSim simulator in Xilinx environment for various test inputs. The simulation results are then presented. | |