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| **Abstract:** |  |
| Abstract— SOI-MOSFET is a candidate for next generation integrated circuit technology due to its reduced junction capacitances and improved subthreshold swing. However, to utilize the technology for circuit application, a robust  circuit model is needed. A complete surface-potential based fully depleted SOI-MOSFET model for circuit simulation has been developed by our group and is named HiSIM-SOI [1, 2]. This model considers device features explicitly as well as preserves the charge conservation. To improve HiSIM-SOI for real application is the purpose of this present work. | |