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| **Title:** | Evolution of Novel Device Structures of MOSFET | | |
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| **Published Journal Name:** | Proceedings of the National Conference on Electronics and ICT | | |
| **Type of Publication:** | Abstract | | |
| **Volume:** | - | Issue | - |
| **Publisher:** | Bangladesh Electronics and Informatics Society | | |
| **Publication Date:** | 20 April 2017 | | |
| **ISSN:** |  | | |
| **DOI:** |  | | |
| **URL:** | https://www.researchgate.net/publication/316349464\_Evolution\_of\_Novel\_Device\_Structures\_of\_MOSFET | | |
| **Other Related Info.:** | p. 20 | | |
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| **Abstract:** |  |
| This talk is about the evolution of novel device structures of MOSFETs since its invention in 1959. Microelectronics has become the cornerstone of computing, communications and consumer electronics revolutions. Of the various microelectronics technologies, Silicon CMOS technology has been driving the integrated circuit (IC) manufacturing industry for more than fifty years. It has been observed that over the years, semiconductor industry has grown faster than general economy of the world, and thus it could attract further investments to fuel and sustain the market growth of this industry through research and innovation for novel device structures of MOSFETs that are needed due to the newer requirements of these industries. The basic requirements are to increase the functionality of MOSFETs without increasing the cost, power and size rather than to decrease it. Hence we need scaling of MOSFETs constantly. But scaling of the device comes with the degradation of the device performance parameters and ultimately circuit performances. Thus the conventional CMOS devices cannot be scaled down much from where they are today because of several device physics limitations, such as, the large tunneling current in very thin gate dielectrics. The classical CMOS structure is reaching its scaling limits at the 35 nm node. That point is often referred to as the ‘end of the road map’ and as such alternative device structures are being investigated. It is shown that alternative device structures can allow CMOS transistors to scale by another 20-25 times. That is as large a factor of scaling as what the semiconductor industry has accomplished in the past. The 1999 International Technology Roadmap for Semiconductor (ITRS), which represents the consensus of the world semiconductor companies on the future of the semiconductor technology, gives clear projections of the device technology up to 0.1 m and recognizes the importance of the alternative structure devices and calls them ‘advanced non-classical CMOS devices’. Beyond that, it is stated that there are no known solutions due to uncertainties about the feasibility of the projected gate dielectric thickness, power supply voltage, substrate doping concentration, dopant density fluctuation, etc. These uncertainties are symptomatic of the general misgivings about the viability of further long-term CMOS device scaling. There will be many opportunities and challenges in finding novel device structures and new processing techniques, and in understanding the physics of future devices. In order to eradicate the problematic scaling issues, device engineers have started transitioning from the conventional planar bulk MOSFET toward the revolutionary novel structures with new materials to get the improved performances like better threshold voltage control, sub-threshold swing, power consumption, flicker noise, noise margin, mobility, operational frequency, bandwidth, propagation delay, speed-power product etc. The novel and alternative structures of MOS devices along with their advantages as well as few application areas of these novel structures are demonstrated in this talk. Finally, few possible research areas are suggested on these new structures with the possibilities of few more structures and materials for the MOS devices. | |