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| **Title:** | A Threshold Voltage Model for sub-100 nm Pocket Implanted NMOSFET | | |
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| **Abstract:** |  |
| Abstract— Pocket implantation is a very useful technique to suppress short channel effects in submicrometer MOS devices. This paper presents a threshold voltage model of pocket implanted sub-100 nm nMOSFETs. The proposed model is derived using two linear equations to simulate the pockets along the channel at the surface from the source and drain edges towards the center of the MOSFET. The threshold voltage equation is obtained by solving the 1D Poisson's equation and then applying Gauss's law at the surface. The model has a simple compact form that can be utilized to study and characterize the pocket implanted advanced ULSI devices. | |