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| **Title:** | Design Steps, Simulation, and Analysis of a 1-bit ALU in Cadence at 90 nm CMOS Node | | |
| **Author(s) Name:** | Kamrul Islam Shohail, Wajiha Awsaf, Saniat Uddin Sayel, Mahabuba Khanam Nitu, and Muhibul Haque Bhuyan | | |
| **Contact Email(s):** | muhibulhb@aiub.edu | | |
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| **Abstract:** |  |
| Abstract— This paper presents the design and analysis of a 1-bit Arithmetic Logic Unit (ALU) with and without a full adder circuit. The objective of the study is to compare the outputs of the two designs considering the performance factors of delay, power, and surface area. The designs were implemented using Cadence Virtuoso and simulated using a 90 nm CMOS process technology. As such, the circuit is built from two paired MOS transistors (i.e., using both N- and P-type MOSs in the pull-down and pull-up circuits, respectively) having a 90 nm gate length. The gate widths are selected as 1 and 2 m, respectively. Transistors are nominated from the general design CMOS process kit at 90 nm technology node, i.e., gpdk090 library of the Cadence. DC, transient, and noise analyses were performed with a 3.8 V DC power supply to characterize the behavior of the circuits. The results indicate that the ALU without the full adder has lower delay and power consumption but a larger area, while the ALU with the full adder has higher delay and power consumption but a smaller area. The findings of this study can provide insights for designers to choose the appropriate ALU design based on their specific requirements and provide a confidence boost before going into the fabrication steps. | |