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| **Title:** | Design, Simulation, and Analysis of Different Operational Factors of a 4-bit Carry Look-Ahead Adder Circuit in Microwind at Several CMOS Technology Nodes | | |
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| **Abstract:** |  |
| Abstract— In Very Large Scale Integration (VLSI) technology, the main objective is to shrink the area and thereby to raise the packing density for performance improvement in terms of power consumption, noise, delay, operating frequency, etc. A carry look-ahead adder circuit is an important block in any digital circuit. It improves the parallel addition process. Since the number of bits in various digital circuits is being increased, as such, we need millions of transistors to perform several functions in parallel. But it increases the need for surface area, power consumption, noise, and other factors. Therefore, we need to reduce the transistor size to alleviate these problems. In this research article, we designed a 4-bit carry look ahead full adder circuit at several technology nodes using Proteus and then simulated it in Microwind. The designed circuit and layout are presented here. Besides, various operational factors are obtained to observe the benefits of the transistors’ size decrement. The layouts are converted and simulated at130 nm, 90nm, 65nm, and45nm CMOS technology nodes. From the comparative analysis, we observed that the reduction of CMOS technology node increases the performance factors of the designed carry look-ahead adder circuit. | |