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| **Abstract:** |  |
| Abstract— The size of CMOS technology is being continuously scaled down in the nano scale regime. But the Boltzmann’s electron distribution creates a major obstacle to it and causes to reach a limit, i.e., the sub-threshold slope value of 60mV/decade attainable at normal room temperature. Reduction of power consumption has become a critical challenge for computational circuits and thus restricts the processing speed of data rate. Negative capacitance transistor proposes to break this limit of SS further down. A Negative Capacitance Field Effect Transistor engages a ferroelectric material in the gate region of the device structure and thus provides an effect of negative capacitance. As such  internal voltage amplification occurs and thereby reduces the sub-threshold slope. In this paper, construction and the physics based working theory behind the NCFET structures, motivation towards the research works on NCFET and their comparative attainment etc. will be discussed and reported elaborately. | |