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| **Title:** | Design and Simulation of a Low Power and High-Speed 4-Bit Magnitude Comparator Circuit using CMOS in DSch and Microwind | | |
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| **Abstract:** |  |
| Abstract— In this paper, we explained how to develop a 4-bit comparator circuit at the Complementary Metal Oxide Semiconductor (CMOS) technology nodes of 90 nm, 65 nm, and 45 nm, draw the logic diagram from the Boolean expression, and the truth table of the logic circuit, find the layout diagram, simulate the voltage vs. time diagram, obtain a 3-D view of the designed circuit, etc. At first, we designed a 4-bit magnitude comparator circuit in DSch with 8 inputs and 3 outputs. After that, we created compilation codes for the Microwind tool to observe the layout diagram for the designed 4-bit comparator circuit. Then we showed the basic operation of a 4-bit comparator circuit and generated the output characteristics curves and determined the surface area requirement, propagation delay, and power dissipation of the circuit. Based on the performance comparisons at various nodes through the simulation results, we revealed that the reduction of the technology nodes improves the circuit performance in terms of these parameters. | |