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| **Title:** | Carrier Conduction Time Delay Model of the Pocket Implanted Nano Scale n-MOSFET | | |
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| **Abstract:** |  |
| Abstract— In this paper, an analytical carrier conduction time delay model in the subthreshold regime of the symmetric pocket implanted nano-scaled n-MOSFET has been presented. The model is developed using the inversion layer charge and subthreshold drain current model for pocket implanted n-MOSFET. The model incorporates the linear pocket profiles symmetric both at the source and drain sides. The linear profiles are then converted into the effective doping concentration by mathematical integration along the channel. Electron current density per unit area is obtained from the conventional drift-diffusion equation in the subthreshold regime. Then inversion channel charge density per unit area is calculated for the pocket doped channel. Thus, the conduction time delay is found in the subthreshold regime. The simulation is carried out for different pocket profiles and device parameters as well as for various bias voltages. The results show that the derived model can produce the conduction delay time in the subthreshold regime that can be utilized to study and characterize the pocket implanted advanced ULSI devices. | |