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| **Title:** | Linear Pocket Profile Based Threshold Voltage Model for NMOSFET down to 50 nm | | |
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| **Abstract:** |  |
| Abstract— The conventional threshold voltage model is derived for the homogeneous doping concentration. As the channel length of MOSFETs is scaled down to a deep-sub micrometer or sub-100 nm regime, we observe short-channel effects, such as steep threshold voltage roll-off, increased off-state leakage current, and bulk punch-through. The short channel effects arise as a result of two-dimensional potential distribution and high electric fields in the channel region. Lateral channel engineering utilizing halo or pocket implant surrounding drain and source regions is effective in suppressing short channel effects. An extension of the homogeneous model to the non-homogeneous impurity pileup in the vertical direction has been reported previously. However, the reported model cannot be extended further to the pocket implantation, where inhomogeneity along the channel is the main cause of the reverse short channel effect (RSCE). A strong reverse short-channel effect suppresses the short-channel effect on the threshold voltage of the MOSFET. Another threshold voltage model for pocket implanted MOSFETs with resolving circuit simulation based on a simplified pocket implanted profile does not describe the case of sub-100 nm. Extrapolation of the threshold voltage versus gate length curve cannot predict the threshold voltage accurately. Therefore, we propose a threshold voltage model that describes the threshold voltage for the gate length down to 50 nm. Advanced MOSFETs are non-uniformly doped because of complex process flow. Therefore, one of the key factors to the modeling threshold voltage (Vth) accurately is to model the non-uniform doping profile of the MOSFET. The focus here is to transform the lateral 1-D pocket profile across the channel into an effective doping concentration expression that can be applied directly to the Vth expression incorporating the Vth shift due to the short channel effect in the model to suppress the short channel effect. This paper presents a threshold voltage model for pocket implanted sub-100 nm NMOSFET. The proposed model is derived using two linear equations to simulate the pocket profiles along the channel at the surface from the source and drain edges towards the center of the MOSFET. An expression for the threshold voltage is obtained by solving the 1-D Poisson’s equation and incorporating effective carrier concentration along the channel. There are other pocket profiles found in the literature, such as Gaussian distribution, hyperbolic cosine profile, etc. for the threshold voltage model of the MOS devices. Our simulation results are compared with the simulation results using these pocket profiles for various device and pocket profile parameters. The comparison shows that the proposed model has a simple compact form that can be used to study and characterize the pocket implanted advanced ULSI devices down to 50 nm gate length. It also proves the validity and usefulness of our proposed model of the threshold voltage for circuit simulation. | |