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| **Title:** | Design Process, Simulation, and Analysis of a Common Source MOS Amplifier Circuit in Cadence at 45 nm CMOS Technology Node | | |
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| **Abstract:** |  |
| Abstract— This work describes a design process, simulation, and analysis of a CMOS-based common source amplifier circuit in the Cadence Virtuoso environment at the 45nm technology node. The suggested CMOS circuit may be useful in the op-amplifier or other circuits. The circuit is designed to work with a 1.8V DC power source. The circuit is constructed from two complementary NMOS and PMOS transistors having a 45 nm gate length. The gate widths are chosen as 1 and 2 m, respectively. Transistors are selected from the gpdk045 library of the Cadence. For the simulation purpose, we have used two sources from the *AnalogLib* library- one is a DC bias source and the other is a pulse source for the input signals. After designing the circuit, the circuit was simulated to test and assess various performance factors, including gain, phase margin, gain bandwidth, power dissipation, etc. Simulation results confirm that the designed circuit works well at this node. This type of design and simulation experience can give confidence to fabrication engineers regarding its functionality and  reliability. | |